Journal on Recent Technologies in Mechanical and Electrical Engineering
Volume: 5 Issue: 6

ISSN: 2349-7947
42 - 44

Reduce Harmonics in Single Phase 28- Echelon Cascaded Multilevel Inverter with Filter

Ram Swaroop[1] Mukesh Kumar Kuldeep[2]
[1,2]Department of Electrical Engineering,
Shekhawati Institute of Engineering & Technology, Sikar, Rajasthan, India

***Abstract*—** This work proposed to cascaded H-bridge multilevel inverter output voltage level is modified and therefore total harmonic Distortion has minimized. Hence this work mainly focused on 27-level cascaded inverter using three H-bridge units. Therefore this method evaluate both single and three phase cascaded H-bridge multilevel inverter reduced specific harmonics and minimized switching loss, electromagnetic interference, and the output voltage gives low total harmonic distortion. In this cascaded multilevel inverter used one separate power source for each H-bridge unit. It was present required multilevel voltage output wave from, the cascaded multilevel inverter topology can overcome some of its limits the conventional method and modified the output voltage level of 13-level cascaded multilevel inverter. This work proposed also used filter circuit to minimize a high amount of harmonics.

Keywords—*Multilevel Inverter, Matlab 12b, AC and DC Voltage, Cascaded Connection*

*****

INTRODUCTION

A cascaded H-bridge multilevel inverter consists of a series of single phase fully H-bridge inverter units. The main aim of this cascaded multilevel inverter is to synthesize a desired voltage from many isolated DC voltage sources from transformer secondary, which can be obtained from batteries, fuel cells, or star cells. Figure shows the fundamental block diagram of a single phase cascaded multilevel inverter with isolated DC voltage sources. Every isolated DC voltage source connected to an H bridge inverter unit. The AC terminal voltages of varied level inverters are connected in series. The cascaded multilevel inverter doesn't requires any voltage leveling capacitors and clamping diodes, in contrast to the flying capacitors and diode clamp inverter.

Among 3 kinds of methodology, the projected methodology is cascaded H-bridge multilevel inverter method. In this technique, the diode clamps the voltage across the switch to 1 level, and all diodes are chosen as same kind i.e. same voltage withstanding capacity. The diode provides the forward path and feedback path in case of the current.

I. LITERATURE SURVEY

As perC. Gnanavel et al [1] , cascaded H-bridge multilevel inverter have an attracted a good deal of attenuation in numerous applications like that medium voltage and high power, owing to their less switching losses, electromagnetic interference, and high efficiency. Among the many cascaded inverters topology it's a lot of attractive owing to the simplicity of control. Author has projected to cascaded H-bridge multilevel inverter output voltage level is reduced total harmonic Distortion. Therefore the author primarily targeted on fourteen level cascaded inverterexploitation3 H-bridge units. Thus that technique appraises each single and 3phase cascaded H-bridge construction electrical converter reduced specific harmonics and reduced shift loss, the output voltage provides low total harmonic distortion.

Kavousi, BehroozVahidi, et al.[3], the author applying bee optimization technique for cut back harmonic within the cascaded H-bridge multilevel inverter. This algorithmic rule is employed to solving the non-linear equations for seven levels H-bridge inverter. The foremost function of this algorithm is reducing low-order harmonics by making use of non-linear equations, whereas the basic part is satisfied. This algorithm is functioning based on the food foraging behavior of a crowd of a honeybees and it complete a neighborhood find combined with a random search. This algorithm has a lot of accuracy and chance of convergence than the genetic algorithm. For the optimization and similitude of genetic algorithm and bee algorithmic rule the MATLAB software system is employed and therefore the results of simulation provides excellence of bee algorithm over genetic algorithm in receiving actual universal minima and supreme convergence rate. Also, this algorithm performance in 10 times run is that the same as in the one-time run, for confirming this, an experimental study was performed.

Zhengming Zhao et al [4], a hybrid Selective Harmonic Elimination Pulse width Modulation (SHEPWM) concept for common mode voltage reduction in three-level neutral-point-clamped inverter-based induction motor drives. The concept uses the traditional Selective Harmonic Elimination Pulse width Modulation (C-SHEPWM) to regulate the inverter at high frequency (≥ 0.9 motor rated frequency) and uses the modified Selective Harmonic Elimination Pulse width Modulation (M-SHEPWM) to regulate the inverter at low frequency. It additionally uses a concept to confirm the sleek transition between the 2 selective harmonic elimination pulse width modulation schemes. As a result, at high frequency, the traditional selective harmonic elimination pulse width modulation provides the specified high modulation index for the motor, whereas at low frequency

DeepaliYadav et al[10],In this article, the output voltage THD of the inverter has been reduced for both balanced and unbalanced configurations using Particle Swarm

ISSN: 2349-7947
42 - 44

Optimization (PSO) method. The proposed approach is an evolutionary and simple robust stochastic search procedure which overcomes the restrictions of Resultant Theory and Newton Raphson method. In this paper, simulation results for ll-Ievel and 13- level CMLI have been presented. These results display that the proposed PSO method is capable of mitigating the harmonic content to as low as 3.87 % for 13-level CMU and 4.43 % for ll-Ievel CMU. The results have been confirmed using MATLAB and harmonic spectrum analysed using Fast Fourier Transform (FFT) window.

II. PROPOSED WORK & RESULTS

The introduced system explication the frequency spectrum and handle the voltage. By using the conduction angle control, minimized the Lower Order Harmonics (LOH). By adjusting the depend upon angle to different echelons, it is possible to better the efficiency and power factor and minimized the lower order harmonics. The Fourier transform is also used to produce the output voltage of multilevel inverter.

The simulation results of single phase and three phases for the developed 14-echelon cascaded multilevel inverter proposed to minimize the total harmonic distortion with using of reduced number of switches and increase level in the output voltage waveform. There are connected three H-bridge inverters in the cascaded form and each H-bridge inverter is supplied by separate DC voltage source. The ratio of the separate DC voltage sources (Vdc1, Vdc2 and Vdc3) that used in single phase and three phase 14-echelon cascaded H-bridge multilevel inverter, as given by-

Vdc1: Vdc2: Vdc3 = 1Vdc : 2Vdc : 3Vdc

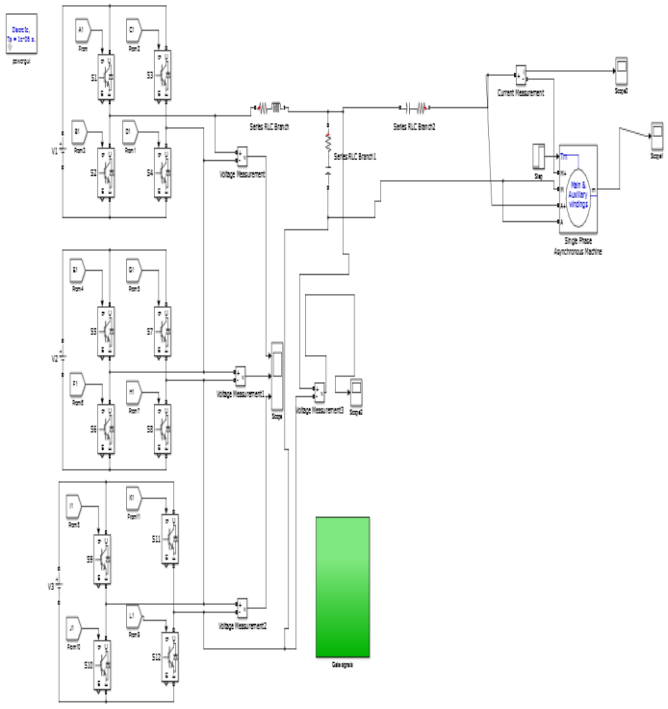

Fig.I-Echelon Cascaded H-Bridge Multilevel Inverter with filter and Load

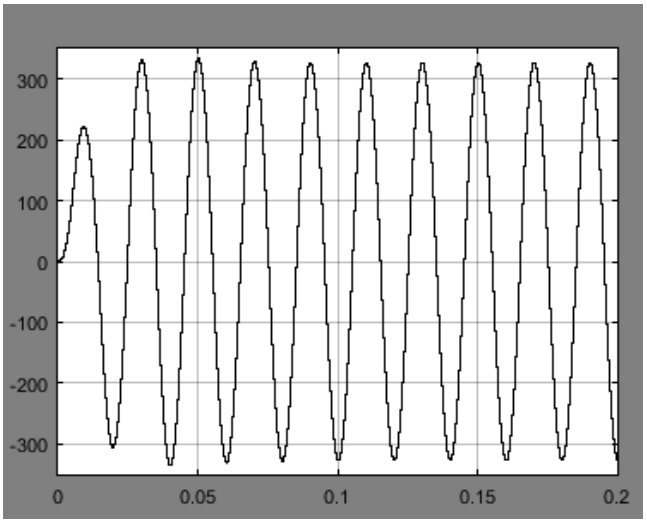

Fig II-.Simulation Output Voltage Waveform for Single Phase 28-Echelon MLI

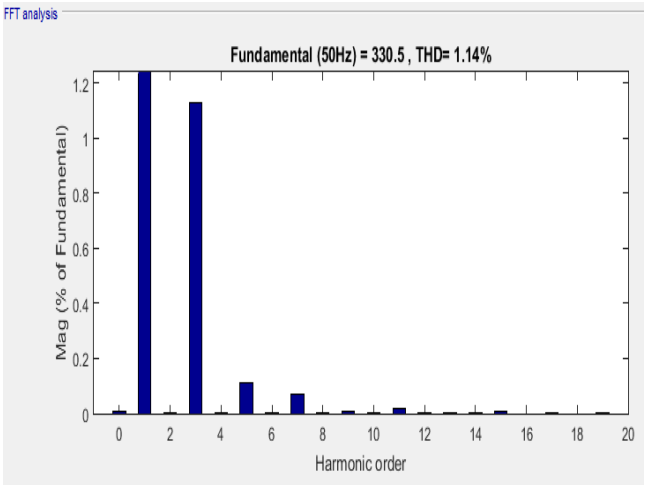

Fig III- FFT Analysis for Single Phase 28-Echelon MLI

Figure-II show the simulation output voltage waveform for single phase 28-echelon cascaded H-bridge multilevel inverter with filter and load and the FFT analysis of that voltage waveform shown in Figure 5.14.The FFT analysis is required to calculate the total harmonic distortion. The simulation result gives the total harmonic distortion level in output voltage for single phase 28-echelon cascaded H-bridge multilevel inverter with filter and load that is 1.14%

References

[1]. C. Gnanavel, N. Kamalamoorthy, V. Prabhu, “Assessment among Single and ThreePhase 14-Echelon Cascaded Multilevel Inverter”, International Journal of Scientific and Research Publications, Volume 3, Issue 5, May 2013
[2]. M. Abolhassani, "Modular Multipulse Rectifier Transformers in Symmetrical Cascaded H-Bridge Medium

ISSN: 2349-7947
42 - 44

Voltage Drives",IEEE Transactions on Power Electronics, vol. 27, no. 2, February 2012
[3]. A. Kavousi, BehroozVahidi, et al., "Application of the Bee Algorithm for Selective Harmonic Elimination Strategy in Multilevel Inverters", IEEE Transactions on Power Electronics, vol. 27, no. 4, April 2012
[4]. Z. Zhao, YulinZhong, et al., "Hybrid Selective Harmonic Elimination Pulse Width Modulation for Common-Mode Voltage Reduction in Three-Level Neutral-Point-Clamped Inverters for Variable Speed Induction Drives", IEEE transactions on power electronics, vol. 27, no. 3, March 2012
[5]. NimaYousefpoor, S. H. Fathi, et al., "Total Harmonics Distortion Minimization Applied Directly on the Line-to-Line Voltage of Multilevel Inverters", IEEE Transactions on Industrial Electronics, vol. 59, no. 1, January 2012
[6]. L.Sabari Nathan,S.Karthik, S.Ravi Krishna "The 27-Level Multilevel Inverter for Solar PV Applications" IEEE 5th India International Conference on Power Electronics (IICPE) 2012 Pages: 1 - 6, DOI: 10.1109/IICPE.2012.6450499
[7]. Y. Ounejjar, Kamal Al-Haddad, and Louis A. Dessaint, "A Novel Six-Band Hysteresis Control for the Packed U Cells Seven-Level Converter: Experimental Validation", IEEE Transactions on Industrial Electronics, vol. 59, no. 10, October 2012
[8]. A. A. KhodadoostArani; H. R. Zaferani; M. J. Sanjari; G. B. Gharehpetian,"Using Genetic Algorithm and Simulated Annealing for 27-level PV Inverter THD Minimization"2014 Smart Grid Conference (SGC) Year: 2014 Pages: 1 - 6, DOI: 10.1109/SGC.2014.7090859
[9]. DeepaSankar; C. A. Babu,"Cascaded H Bridge Multilevel Inverter Topologies for PV Application:A Comparison"International Conference on Circuit, Power and Computing Technologies (ICCPCT) Pages: 1-5, DOI:10.1109/ICCPCT.2016.7530140
[10]. DeepaliYadav; Jagdish Kumar,"Harmonic Minimization Using PSO Technique for CMLI with Unequal and Equal DC Sources"IEEE 1st International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES) Year: 2016 Pages: 1 - 5, DOI: 10.1109/ICPEICES.2016.7853330
[11]. G. Carrara, S. Gardella, M. Marchesoni, R. Salutari, and G. Sciutto, "A New Multilevel Pulse Width Modulation Method: A Theoretical Analysis", IEEE Transactions Power Electronic, vol. 7, no. 3, pp. 497-505, July 1992
[12]. L. M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel Converter for Large Electric Drives"IEEE Transactions on Industrial Electronics, vol. 35, no. 1, pp. 36-44, Jan. 1999
[13]. L.Sabari Nathan, S.Karthik, S.Ravi Krishna "27-Level Multilevel Inverter for Solar PV Applications"IEEE Transactions on Industrial Electronics,978-4673-0934-9/12
[14]. DeepaliYadav, Jagdish Kumar, "Harmonic Minimization Using PSO Technique for CMLI with Unequal and Equal DC Sources",IEEE International Conference on Power Electronics. Intelligent Control and Energy Systems (ICPEICES-2016)