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Estimation of Short Circuit Power Dissipation in CMOS Inverter

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Abstract:- Optimization of high speed CMOS circuit is to discover the variation in physical parameters, which affects the circuit performance. T-sizing is one such method to analyze the parameter variation. A considerable part of energy dissipation in CMOS is due to short circuit currents. The channel length of the transistors is fixed and the size of the transistor is defined by its width. Decreasing the channel length and gate oxide thickness increases transconductance, i.e., the current drive of the transistor. The proposed work is a compact model for the short circuit power dissipation, which deals with the analytical formulation of short circuit power dissipation and also to reduce the power consumption of CMOS inverter. In order to minimize the signal delay the transistor parameters has to be varied accordingly. Dynamic power is taken into considerations because static power is negligible. The energy model presented in this work accounts the influences of input voltage transition time, transistor sizes ,device carrier velocity saturation ,narrow – width effects ,gate drain ,short circuiting transistor's gate source capacitances and output load dissipation using MATLAB software which calculates the voltage and current as a function of time when a large signal is applied.

Keywords—*Delay effects, CMOS inverter, T-sizing, path based optimization, global optimization and short circuit power dissipation.*

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1. INTRODUCTION

Transistor sizing is a timing optimization method in high performance design. The objective is to meet timing constraints by assigning optimal transistor widths,keeping the total transistor area as minimal as possible . Transistor sizing and also gate sizing is an active research topic in recent years[1]. The power consumption of a single static CMOS gate, neglecting the static power consumption, is composed of Pcap, the capacitive power due to charging and discharging of capacitors and Psc, the short circuit power dissipated when both the p-type and the n-type blocks are conducting simultaneously during a transition. The capacitive power is well understood, and is given by

$$\mathbf{P_{cap} = C_L V^2 f} \qquad \textbf{(1)}$$

Process variability is creating daunting challenges for achieving predictable process and product times-to-market with the economically acceptable yield levels[2]. The sources of variability are magnified .when aggressively scaling technology nodes based on the same fundamental device architectures, processes, and layout design styles. Since the computation of the capacitor current is relatively complicated because it requires the calculation of the MOS transistor currents, for propagation delay calculation there is no benefit in calculating the capacitor current twice. A single current calculation, corresponding to the familiar midpoint integration method, is sufficient to get the same or better accuracy as that of the average capacitor current method. The two-point Gauss quadrature formula is shown to provide excellent results with two capacitor current evaluations. In this paper, we introduce a new method that has a number of important advantages over current methods .We formulate the CMOS op-amp design problem as a very special type of optimization problem called a *geometric program*. The most important feature of geometric programs is that they can be reformulated as *convex optimization problems* and, therefore, *globally optimal* solutions can be computed with *great efficiency*, even for problems with hundreds of variables and thousands of constraints, using recently developed interior-point algorithms. Thus, even challenging amplifier design problems with many variables and constraints can be (globally) solved. The fact that geometric programs (and, hence the CMOS op-amp design problems cast as has a geometric programs) can be globally solved number of important practical consequences. The first is that sets of infeasible specifications are unambiguously recognized: the algorithms either produce a feasible point or a proof that the set of specifications is infeasible. Indeed, the choice of initial design for the optimization procedure is completely irrelevant (and can even be infeasible); it has no effect on the final design obtained. Since the global optimum is found, the op-amps obtained are not just the best our method can design, but in fact the best *any* method can design (with the same specifications).In particular, our method computes the *absolute limit of performance* for a given amplifier and technology parameters[3].

2. MOS MODEL

Most of the existing methods assume that the power consumption of a circuit is proportional to the active area" of the circuit. Therefore they assume that minimizing the active area also minimizes the power consumption of the circuit. However, to enable efficient circuits as well as limit the total number of patterns in the design requires a methodology for specifying predefined locations at which selected deviations can be placed[4]. As these deviations are tightly coupled with specific circuit functionality.

2.1 Need for scaling the MOS transistors:

1. Increase device packing density
2. Improve frequency response (transition time) α 1/L
3. Improve current drive (transconductance) gm

$$g_m = \frac{\partial I_D}{\partial V_G} \quad \textbf{at } V_D\textbf{=const} \qquad (2)$$

$$g_m \approx \frac{W}{L}\mu_n \frac{K_{ox}}{t_{ox}} V_D \quad for\ V_D<V_{SAT} \qquad \textbf{(3)}$$

$$g_m \approx \frac{W}{L}\mu_n \frac{K_{ox}}{t_{ox}}(V_G - V_T) \quad for\ V_D > V_{SAT} \qquad (4)$$

Decreasing the channel length and gate oxide thickness increases gm, i.e., the current drive of the transistor. Much of the scaling is therefore driven by decrease in L and tox. However if only these two parameters are scaled many problems are encountered, e.g., increased electric field. In reality constant field scaling has not been observed strictly.

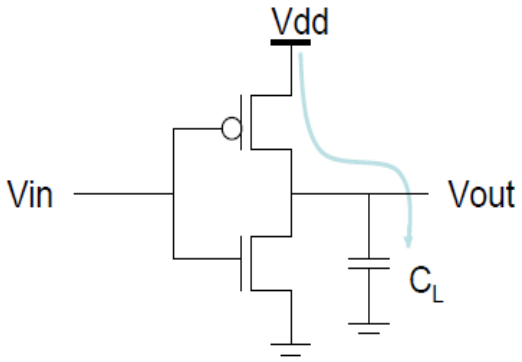

Figure 1 : CMOS inverter

Linear region:

$$I_D = \frac{W}{L}\mu_n C_{OX}'[V_G - V_T]V_D \qquad (5)$$

Saturation region:

$$I_{D_{SAT}} = \frac{W}{2L}\mu_n \frac{\epsilon_{ox}}{t_{ox}}(V_G - V_T)^2 \qquad (6)$$

Since the transistor current is proportional to the gate overdrive (VG-VT), high performance demands have dictated the use of higher supply voltage. However, higher supply voltage implies increased power dissipation (CV2f). In the recent past low power applications have become important and have required a scaling scenario with lower supply voltage.

3. SHORT CIRCUIT POWER CALCULATION:

The short circuit power dissipation, Psc is given by the equation as

$$P_{sc} = \left(\frac{\beta}{12}\right)(v - 2T)^3\left(\frac{\tau}{T}\right) \qquad (7)$$

Here, β is the gain-factor of the transistor, VT is the threshold voltage and τ is the input transition time. T =1/f, is the time period. We assume in the following analysis that the channel length of the transistors is fixed and the size of the transistor is defined by its width. The gain factor, β is proportional to the width of the transistor (p-transistor for a low-to-high transition and n-transistor for a high-to-low transition), W, and the mobility of the carrier (_p for low-to-high, _n for high-to-low). Hence,

$$P_{sc} = k\mu W_\tau \qquad (8)$$

Where $k = c\frac{(v-2v_T)^3}{12T}$,c is a constant of proportionality. v_T is the threshold voltage and v is the supply voltage of the inverter[2]. Thus, the short circuit power consumption is directly proportional to both the width of the transistors and the input transition time.

3.1 Subthreshold Conduction

When the surface is in weak inversion (i.e., o < φs < φp , VG < VT), a conducting channel starts to form and a low level of current flows between source and drain.

3.2 Effect of Reducing Channel Length: Drain Induced Barrier Lowering (DIBL)

In devices with long channel lengths, the gate is completely responsible for depleting the semiconductor (QB). In very short channel devices, part of the depletion is accomplished by the drain and source bias Since less gate voltage is required to deplete QB, VT↓ as L↓. Similarly, as VD ↑, more QB is depleted by the drain bias, and hence VT↓ . These effects are particularly pronounced in lightly doped substrates. If the channel length becomes too short, the depletion region from the drain can reach the source side and reduces the barrier for electron injection. This is known as punch through[5]. In devices with long channel lengths, the gate is completely responsible for depleting the semiconductor (QB). In very short channel devices, part of the depletion is accomplished by the drain and source bias. Since less gate voltage is required to deplete QB, the barrier for electron injection from source to drain decreases. This is known as drain induced barrier lowering (DIBL).

3.3 Effect of Reducing Channel Width on VT

There are no diffusions on the side of the channel. Hence the depletion region extends sideways in areas lying outside the gate controlled region increasing the apparent channel width. As a result the VT is increased. Note that the effect here is opposite to that of reducing channel length.

4. OUTCOMES

The model is validated for CMOS Inverter in the figures shown below ,the short circuit energy per transition is plotted for different input transition times ,capacitive loads and inverter sizes. The results shows a very good agreement with MATLAB software .

In addition ,the graph gives a short circuit energy per transition is plotted a as a function of the range of supply voltage applied in modern CMOS circuits . Thus the power consumption of CMOS inverter is also reduced in such a manner area of the transistor is minimized by increasing speed of the chip with a minimum propagation Delay .

The parameter variations are plotted as shown in the following figure 2,3,4

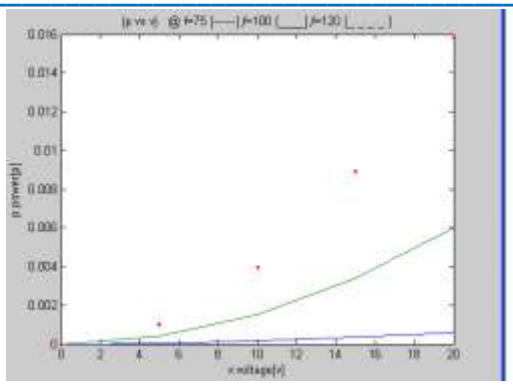

Figure 2: Power Delay Product

For the variation of frequency such as f=120[-------] , f=100[___], f=75 [.....]

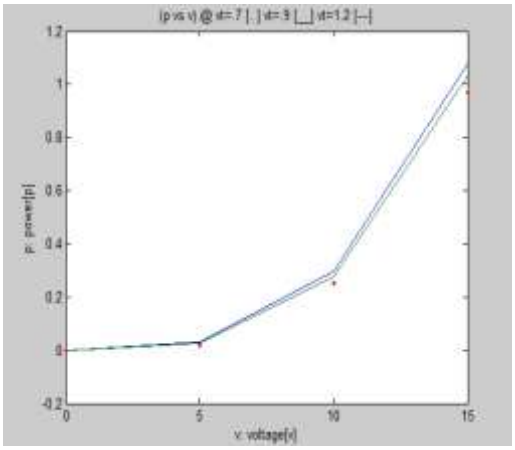

Figure 3: Short Circuit Power Dissipation

For the variation of Threshold voltage such as Vt=0.7[.....], Vt=0.9[----], Vt=1.2[__]

Figure4 displays another interesting fact. Here we have started with 3 different initial solutions, one with 90% of the allowable range of the widths, another with 75% and the last one with 60% of the allowable width range. All of them appear to converge in more or less the same region of the slack/area space.

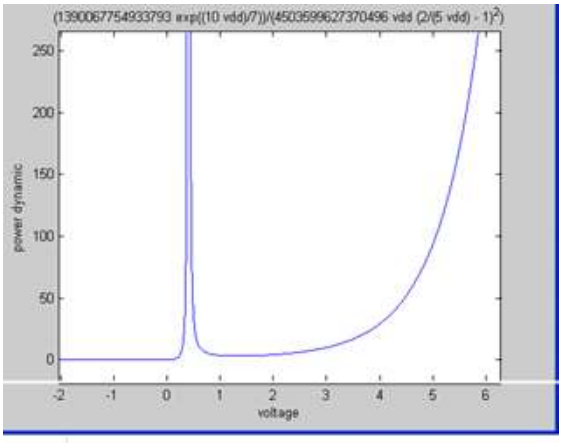

Figure 4: Dynamic Power

We have run experiments on several real circuits under very tight timing constraints. In all the experiments, we have chosen an initial solution where all the transistors are assigned a width of 75% of their allowable range. The result shows that the proposed algorithm is capable of yielding better result than Focus, in terms of best slack, area or both. Even in cases when it cannot beat Focus result it comes very close to Focus Best Solution. Also the runtime in general appears to be much better than that of Focus.

5. CONCLUSION

As a conclusion , the presented energy model accounts for the influences of input voltage transition time, transistor sizes, device carrier velocity saturation and also the narrow – width effects ,gate drain and short circuiting transistor's gate source capacitances ,output load and provides an analytical and accurate method for the evaluation of the short circuit energy dissipation in CMOS Inverters.

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