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Design and Performance Analysis of Arithmetic Circuits using Hybrid CMOS Logic and GDI Based Full Adder

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Abstract - The Full Adder circuit is an important component in many applications such as Digital Signal Processing architecture, microprocessor, and microcontroller and data processing units. Two new designs have been adopted in order to create full adders to obtain low power, reduction in delay and area parameter. Those two new designs are Hybrid CMOS logic style and Gate Diffusion Input Structure (GDI).

Then the modified full adders will be inserted in arithmetic circuits such as carry save adder and carry save array multiplier. The designs will be simulated using T-Spice tool to analyse the performance in terms of area, delay, power and Power Delay Product. These designs successfully will operate at low voltages with tremendous signal integrity and driving capability when compared with the conventional full adders.

Keywords— Hybrid Logic style, Gate-Diffusion Input, Area, Power, Delay and Power-Delay Product

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I. INTRODUCTION

The main design challenge to be addressed will be the power consumption. Smaller the area smaller will be the power consumption. In general it depends on number of logic gates used inside the circuit. Therefore reducing power has a direct impact in reduction of area. The adder improves delay with increase in parallelism. If the propagation delay of the adders is less at each stage then the delay of the adder is reduced. This becomes a great challenge when it comes for a larger bit value. Reducing delay without disturbing the other parameters is quite an impossible case in which each value depends on the other value which is a major concern.

II. DESIGN OF MODIFIED FULL ADDERS

Two modified full adders have been designed in order to implement those in arithmetic circuits to reduce performance parameters like area, power, delay and its product.

A. Modified Hybrid Full Adder

The modified hybrid full adder is a Low Power full adder, which has good characteristic in terms of speed and power [1]. This design is based on Semi XOR-XNOR gates but it has lack of ability to generate all the possible outputs as in conventional XOR-XNOR gates as it can be inferred from the Table I.

TABLE I
TRUTH TABLE OF SEMI XOR AND SEMI XNOR GATE

A	B	Semi XOR	Semi XNOR
0	0	0	Z
0	1	1	0
1	0	1	0
1	1	Z	1

As can be seen from the Table I, the SEMI XOR gate has the ability to generate the first four states of the sum output, with the remaining states produced with the Semi XNOR gate. From Table II, in order to design the Sum circuit, these Semi XOR-XNOR gates could be employed with C_{in} input which is used as a selector. When C_{in} is equal to '0', the Semi XOR gate is similar to the Sum, and when C_{in} is equal to '1', the Semi XNOR gate is similar to the remaining states of the Sum [4].

The high impedance states would cause a malfunction in the circuit. One of these two situations occurs when 'A' and 'B' inputs are equal to '1' and C_{in} input is '0'. In order to have the correct value at the output node, we have to add one more transistor to compensate for the inability of the presented circuit in this specific state [4].

TABLE III

Cin	B	A	Sum	C	Semi XOR	Semi XNOR
0	0	0	0	0	0	Z
0	0	1	1	0	1	0
0	1	0	1	0	1	0
0	1	1	0	1	Z	1
1	0	0	1	0	0	Z
1	0	1	0	1	1	0
1	1	0	0	1	1	0
1	1	1	1	1	Z	1

If we connect the output of the Semi XNOR gate to the gate of one NMOS transistor, where the source or drain of this transistor is connected to SUM output and its drain or source is connected to the C_{in}, the high impedance states in the output will be set to the appropriate value. It is significant to know that this newly added NMOS transistor can be turned on in two situations when the output of Semi XNOR gate is equal to '1', where the output of the SUM in these two states is equal to the C_{in} [1]. So by connecting the C_{in} to the drain/source of this NMOS, there would be no adverse effect to the circuit functionality. Complete design of the modified full adder is shown in Fig. 1 below [1].

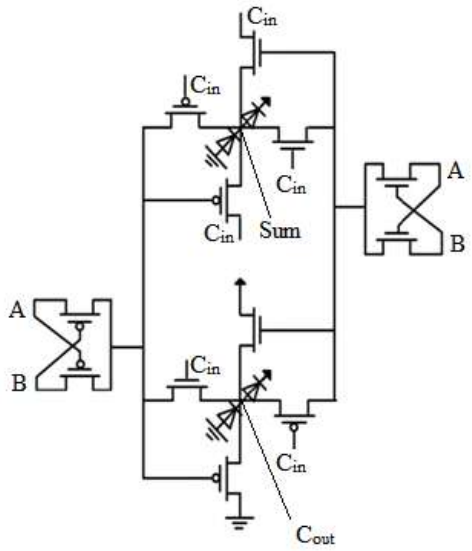

Fig. 1 Modified Hybrid Full Adder [1]

B. *Gate Diffusion Multiplexer Full Adder*

This approach for designing full adder eliminates the need for complicated XOR-XNOR gates. From table 4.2 it can be seen that C_{out} is equal to (A . B) when C_{in}='0', and C_{out} is equal to (A + B) when C_{in}='1'. Thus a multiplexer can be used to obtain the C_{out} output. Following the same criteria, the SUM output is equal to (A + B + Cin) when C_{out}='0', and SUM is (A . B . Cin) when C_{out}='1'. Again, C_{out} can be used to select the respective value for the required condition, driving a multiplexer. An alternative logic scheme to design a full adder cell can be formed by AND, OR and MUX logic blocks which is shown in Fig. 2.

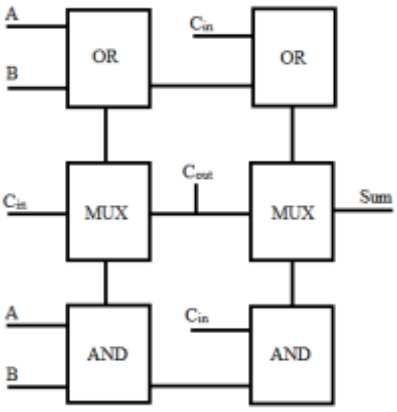

Fig. 2. Logic Scheme for Designing Full Adder [1]

To implement this logic scheme GDI technique is used. It contains three inputs. G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS). Bulks of both NMOS and PMOS are linked to N or P, so it can arbitrarily be biased at contrast to a CMOS inverter. These features give the GDI cell two extra input pins to use, which makes the GDI design more flexible than usual CMOS design [1]. It must be remarked that not all of the functions are possible in standard p-well CMOS process but can be successfully implemented in twin-well CMOS or silicon on insulator (SOI) technologies. This technique allows reducing power consumption, propagation delay and area of digital circuits while maintaining low complexity of the design. The GDI technique allows use of simple and efficient design algorithm, based on the Shannon expansion [2]. It makes the GDI suitable for synthesis and realization of combinatorial logic in real LSI chips, while using a single library.

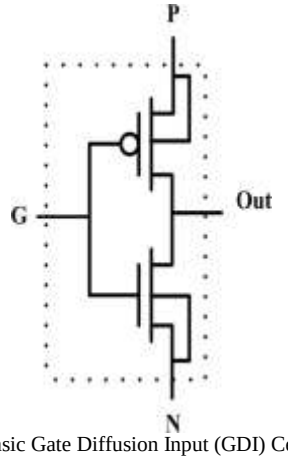

Fig. 3. Basic Gate Diffusion Input (GDI) Cell [2]

III. Implementation Of The Modified Full Adders In Arithmetic Circuits

A. *Carry Save Adder*

The important point to note is that sum and carry can be computed independently. Carry out can be saved instead of using it immediately to calculate the final sum. There are many cases where it is desired to add more than two numbers together. The straightforward way of adding together 'm' numbers is to add the first two, then add that sum to the next, and so on. This requires a total of 'm – 1' additions, for a total gate delay of O (m log n). Instead, a tree of adders can be formed, taking only O (log m ·log n) gate delays. Structure of a two bit CSA is shown in figure 4 below.

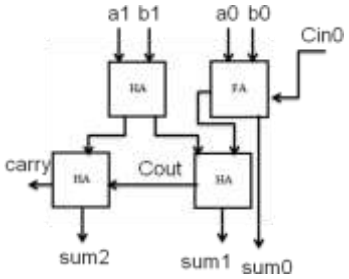

Fig. 4. Conventional Carry Save Adder

Instead of using conventional full adder, modified hybrid CMOS logic style and GDI based full adders have been inserted and compared with the existing carry save adder which is shown in figure 4.

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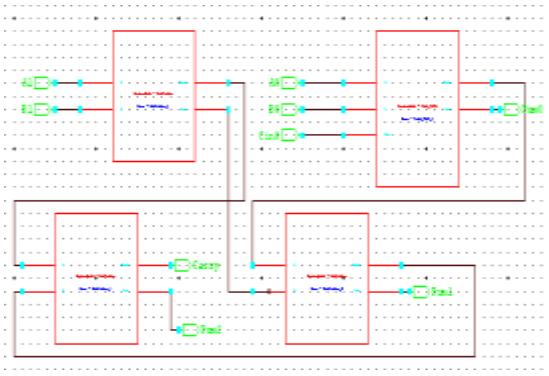

Fig. 5. Modified Full Adder based Carry Save Adder in S-Edit

B. Carry Save Array Multiplier

Multipliers play an important role in today's digital signal processing and various other applications. With advances in technology, many researchers have tried in designing multipliers which offer any of the design targets. They are high speed, low power consumption, regularity of layout and hence less area or even combination of them in one multiplier thus making them suitable for high speed, low power and compact VLSI implementation.

With increasing parallelism, the amount of shifts between the partial products and intermediate sums to be added will increase which may result in reduced speed, increase in silicon area due to irregularity of structure and also increased power consumption due to increase in interconnect resulting from complex routing.

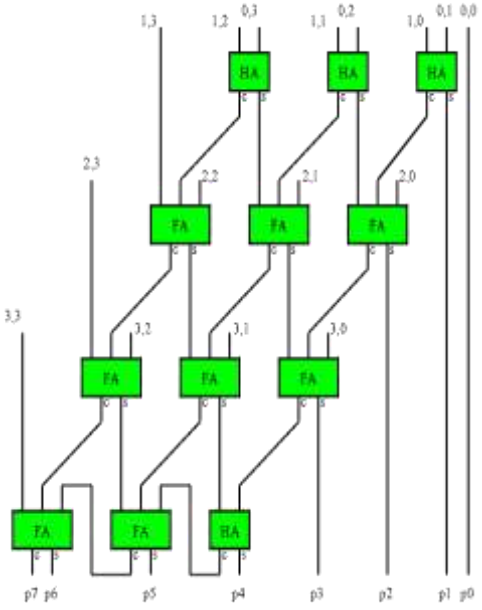

Fig. 6 Design of a Carry Save Array Multiplier

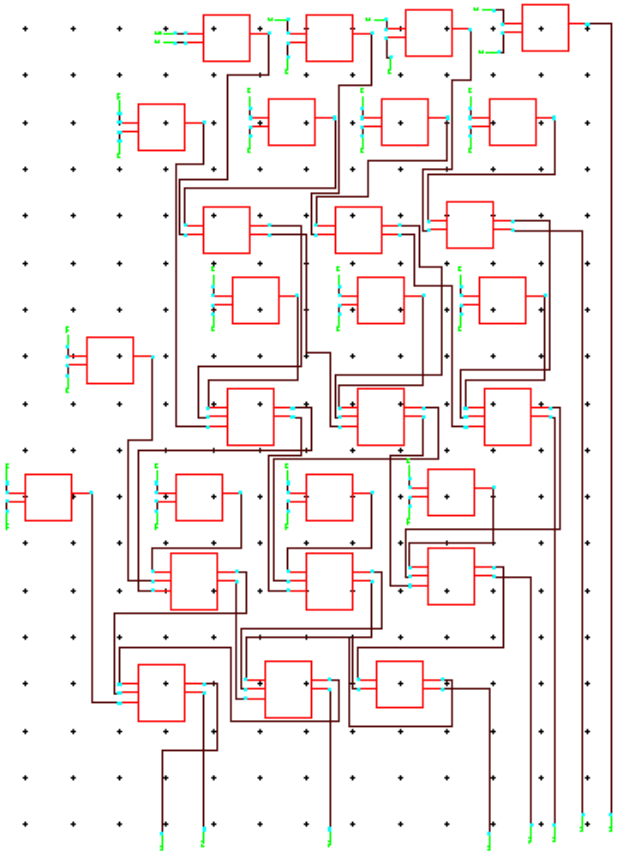

Fig. 7 Modified Full Adder based Carry Save Array Multiplier in S-Edit

IV. SIMULATION RESULTS

The working tool chosen here is T-Spice. With key features such as multi-threading support, device state plotting, real-time waveform viewing and analysis, and a command wizard for simpler SPICE syntax creation.

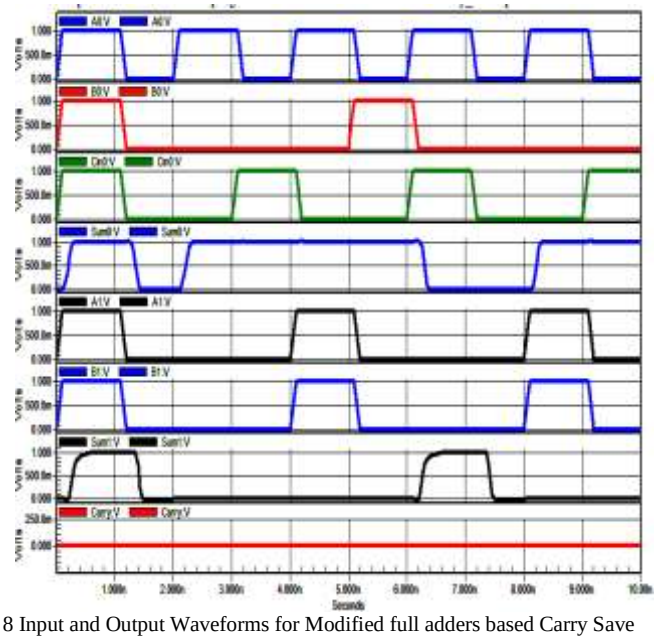

Fig. 8 Input and Output Waveforms for Modified full adders based Carry Save Adder

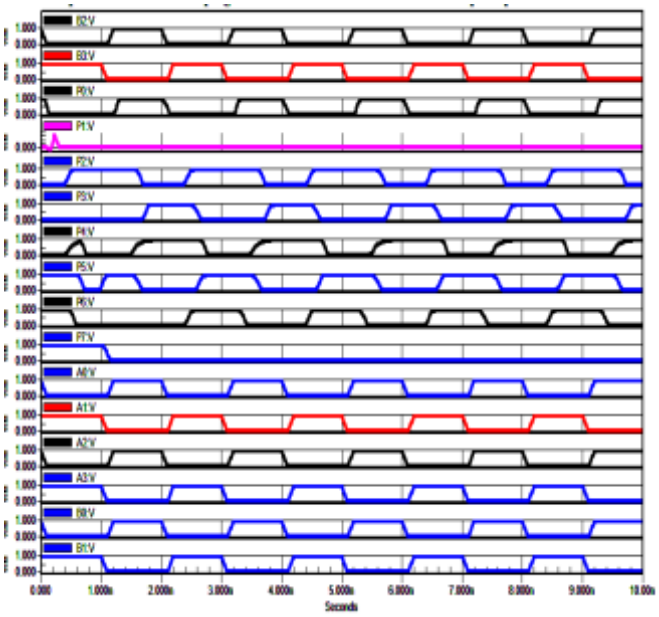

Fig. 9 Input and Output Waveforms for Modified full adders based Carry Save Array multiplier

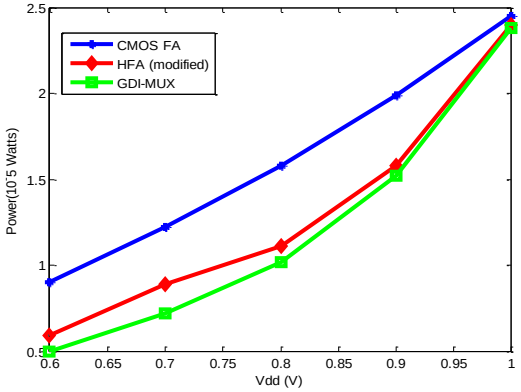

Fig. 10 Power results for modified full adder based Carry Save Adder at different supply voltages

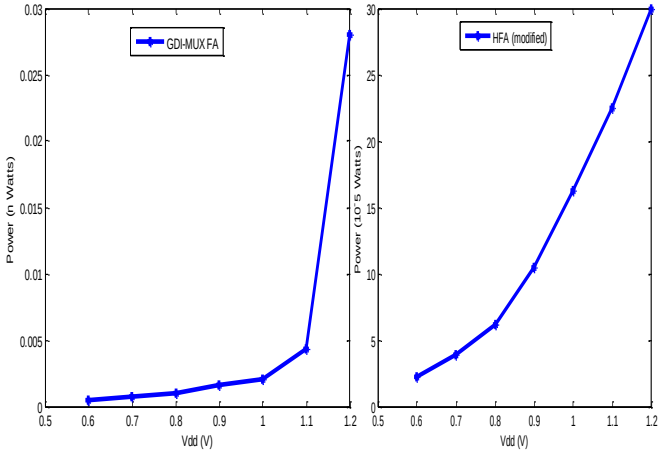

Fig. 11 Power results for modified full adder based Carry Save Array multiplier at different supply voltages

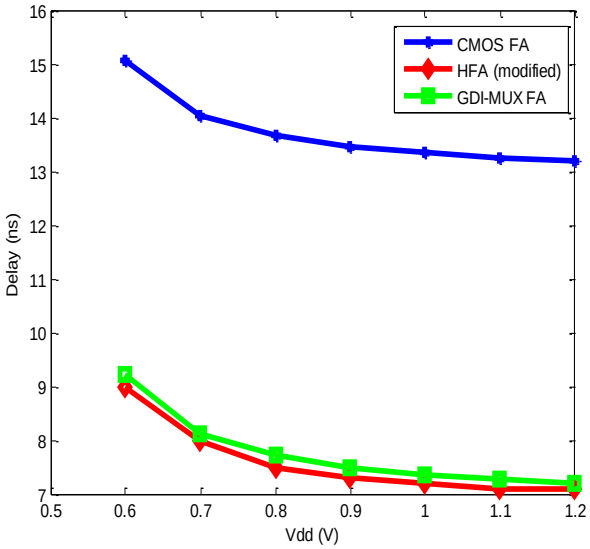

Fig. 12 Delay results for modified full adder based Carry Save Array Multiplier at different supply voltages

V. CONCLUSIONS

In terms of area, the modified hybrid full adder and GDI MUX full adder with 20 transistors have the smallest area because of the symmetric arrangement in its design. The GDI MUX full adder shows the minimum power consumption at all supply voltages when compared with the other adders. The modified hybrid full adder cell has the smallest delay. When the output load is increased, both modified hybrid full adder and the GDI MUX full adder show the best performance.

In order to have a practical application, the modified hybrid full adder and GDI MUX full adders have been implemented in cascaded full adders like ripple carry adder, carry save adder and in carry save array multipliers. The performance parameters such as power, delay and power delay product have been improved significantly.

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